REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

The present remark is in response to the Office Action mailed November 17, 2004, in which Claims 1 through 30 were rejected. No claims are amended. No Claims are canceled and no claims are added. Accordingly, Claims 1-30 remain pending.

CLAIM REJECTION-35 U.S.C. SECTION 102 (e)

With respect to Page 2 through 4 of the Office Action, Claims 1, 9, 12, 14, 15, and 16 stand rejected under 35 U.S.C. 102 (e) as being anticipated by Lee et al (U.S. Patent No. 6,607,984).

According to the disclosure of Lee et al '984, which discloses the semiconductor memory employing deep trench capacitor technology, the method includes an oxide collar that are formed in trenches, and the trenches filled with polysilicon or equivalent conductive material to form a storage node for the trench capacitor (column 5, lines 58-63). Nevertheless, Lee et al '984 does not disclose the "capacitor is formed in the interior of said opening of said semiconductor substrate" as in claim 1. Lee et al '984 discloses "trenches have been filled with polysilicon or equivalent conductive material to form a storage node for the trench capacitor". Thus, there is no "capacitor" formed in the opening in the disclosure of Lee et al '984.

Moreover, according to the disclosure of Lee et al '984 they do not disclose the step of "removing parts of said insulator layer, said second hard mask layer, said first hard mask layer and said semiconductor substrate, "with a part of said insulator layer as a mask", to form a trench in the middle between partial said two capacitors, wherein a different removing rate exists between said insulator layer and said second hard mask layer". Lee et al '984 discloses a portion of layer 124 is selectively removed relative to layer 122. Layer 122 and pad nitride 115 are also

removed in accordance with the pattern of resist layer 130 (column 6, lines 43-48). Lee et al '984 does not employ "a part of said insulator layer as mask" to form a "trench", and also does not have the trench "in the middle between partial said two capacitors" in the structure of Lee et al '984. Therefore, according to the above reasons, Applicants believe that Lee et al '984 cannot anticipate the present invention. Thus, claims 1, 9, 12, 14, 15, and 16 are patentable over Lee et al. '984 and Applicants respectfully request withdrawal of these rejections.

CLAIM REJECTION-35 U.S.C. SECTION 103 (a)

Claims 2-4, 8, 11,17-18, 21-22, 24-25, and 27-30 stand rejected under 35 U.S.C. 103(a) as being unpatentbale over Lee et al '984 as above in view of Wensley et al (U.S. Patent No. 6,566, 227).

Examiner is of the opinion that Wensley et al '227 teach filling a STI region with an oxide, as well as the depths of the deep trench (DT) and shallow trench in a DRAM device. Nevertheless, the formation of the "trench" is different. In the claimed invention, the step is "removing parts of said insulator, said second hard mask layer, said first hard mask layer and said semiconductor substrate", "with part of said insulator layer as mask", to form a trench in the middle between partial said two capacitors,...". In Wensley et al '227, the formation of the trench is the pad nitride and first semiconductor material are patterned with trenches, e.g., deep trenches (DTs). Wensley et al '227 does not disclose the part of insulator layer as mask and also does not disclose a different removing rate exists between said insulator layer and said second hard mask layer. Therefore, Applicant believes that the combination of the disclosure of Lee et al ' 984 in view of Wenley et al '227 cannot achieve the claimed invention.

Claims 5-7, 10, and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentbale over admitted prior art in view of Lee et al '984.

The Examiner is of the opinion that the admitted prior art depicted in FIG. 1A-1D and described in the pending specification in page 2-3 teach substantially the claimed invention. Lee et al '984 teaches a process in which a STI region is etched using a composite hard mask layer of SiO_2/BARC as an etch mask for the etching, wherein a removable rate between said SiO_2 layer and said BARC layer is different. Nevertheless, the claimed invention recites the trench is formed by removing parts of said insulator layer, said second hard mask layer, said first hard mask layer and said semiconductor substrate,..." with "a part of said insulator layer as a mask". The admitted prior art did not employ the "parts of insulator layer as a mask" to induce the misalignment, such that the internal electrode of the left DT capacitor is over etched. Thus, the combination of the admitted prior art in view of Lee et al '984 does not disclose the "with parts of insulator layer as mask" as the claimed invention recites. Thus, Applicants believe that the combination of the disclosure of admitted prior art in view of Lee et al '984 cannot achieve the present invention.

Claims 19, 29, 23, and 26 stand rejected under 35 U.S.C. 103(a) as being unpatentbale over admitted prior art taken with Lee et al '984 as applied to claims above, and further on view of Wensley et al '227 cited above.

Applicants hold that the combination of the disclosure of Lee et al '984 in view of Wensley et al '227 does not disclose the "with a part of said dielectric layer as a mask" to form "a trench in the middle between partial said two capacitors,..." as in Claim 18. Although the admitted prior art taken with Lee et al '984 as applied to claims above, and further on view of Wensley et al '227 have been disclosed the part steps of the claimed invention, nevertheless, the combination of the admitted prior art, Lee et al' 984 and Wensley et al '227 still lacks of the "with a part of said insulator layer as mask" to induce the "misalignment". Thus, Applicants believe that the combination of the admitted prior art, Lee et al' 984 and Wensley et al '227 cannot achieve the present invention.

Conclusion

In the light of the above amendments and remarks, Applicants respectfully submit that all pending Claims 1 through 30 as currently presented are in condition for allowance. Applicants have thoroughly reviewed that art cited and relied upon by the Examiner. Applicants have concluded that these references do not affect the patentability of these claims as currently presented. Accordingly, withdrawal of the rejections and reconsideration is respectfully requested.

Respectfully submitted,
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Date: January 31, 2005 By: Cathi J. G. Thoorsell
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